



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,495	02/11/2002	William A. Stevens, JR.	042390.P9143	6012
7590	08/31/2007		EXAMINER	
Lawrence E. Lycke			CHEN, TSE W	
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP			ART UNIT	PAPER NUMBER
Seventh Floor			2116	
12400 Wilshire Boulevard				
Los Angeles, CA 90025-1026				

  

MAIL DATE	DELIVERY MODE
08/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

5

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/073,495	STEVENS, ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Tse Chen	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A. SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 02 August 2007.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 42-56 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 42-56 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____   | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 42-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). According to Applicant's Remarks dated August 2, 2007, the term "dispatch" in claims 42-56 is used by the claim to mean "execute", while the accepted meaning is "issue a fetched instruction to one or more functional units for execution"<sup>1</sup>. The term is indefinite because the specification does not clearly redefine the term – in one instance, it appears as if dispatch means execute [pg. 9, ll.3-4] while in another instance, at least original claim 1 appears to refer to the accepted meaning with "dispatching the scheduled modules for execution". In order to proceed with prosecution, Examiner will take the position that Applicant intends "dispatch" to be "execute".

### *Claim Rejections - 35 USC § 103*

---

<sup>1</sup> "IEEE 100 The Authoritative Dictionary of IEEE Standards Terms", Seventh Edition, 2000.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 42-44, 48, 50-51, 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens, US Patent 6633976, in view of Patel, US Patent 5999989.

6. In re claim 42, Stevens discloses a method comprising:

- Initializing a plurality of firmware modules [col.2, l.48 – col.3, l.15], wherein the initializing comprises:
  - Examining at least two firmware modules [module to initialize CPU, module to initialize memory] to determine a required order of dispatch of the firmware modules [col.2, ll.59-60; col.3, ll.2-3; examination of modules and determination of required order of dispatch may be coded before runtime].
  - Dispatching an earlier of the two firmware modules and then dispatching a later of the two firmware modules [ordered execution of initialization modules results in one module being the earlier and the other being the later] [col.3, ll.2-3].
- After initializing the plurality of firmware modules, initializing a system memory [system memory is initialized after initialization of modules that includes the module that is to initialize the system memory] [col.3, ll.2-3].

Art Unit: 2116

7. Stevens did not disclose invoking a function contained in a third firmware module during a dispatch of the earlier firmware module or the later firmware module.

8. Patel discloses a method comprising invoking [call] a function contained in a third firmware module [module that starts at 03h for initializing the device] during a dispatch [execution] of the earlier firmware module [e.g., POST] or the later firmware module [col.7, ll.14-16].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Patel before him at the time the invention was made, to modify the system taught by Stevens to include the teachings of Patel, in order to obtain the claimed method and system. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enhance the robustness of BIOS operation [Patel: col.1, ll.51-56; e.g., Patel's teaching enhances Stevens' early initialization by enabling the determination and initialization of different resources] while conserving memory resource [Patel: col.3, ll.40-48; run Stevens core module statically instead of via system memory to conserve memory resource].

10. In re claim 43, Patel discloses, wherein examining comprises checking a resource list of each of the two firmware modules [associated with BIOS] [col.12, ll.7-18].

11. In re claim 44, Patel discloses, wherein the initialization [POST part of initialization] of the plurality of firmware modules comprises examining a platform to determine whether hardware to be initialized by the module is present in the platform [col.14, ll.13-26].

12. As to claim 48, Patel discloses, wherein the third firmware module is dispatched before the function contained in the third firmware module is invoked [col.7, ll.14-16;

firmware module implicitly needs to be dispatched first before function in firmware module can be executed as admitted by Applicant in Remarks dated August 2, 2007].

13. In re claim 50, Stevens discloses a computer-readable medium containing instructions [initialization code] to cause a programmable processor [that runs initialization code] to perform operations comprising initializing a volatile memory [RAM] after dispatching the plurality of firmware modules [module to initialize CPU, module to initialize memory] [col.3, ll.2-3; col.5, ll. 37-39].

14. Stevens did not discuss the details of determining dependencies among a plurality of firmware modules based on information about services imported and exported by each of the firmware modules

15. Patel discloses a computer-readable medium [system ROM] containing instructions to cause a programmable processor [e.g., CPU] to perform operations [col.2, ll.39-49; col.3, ll.40-43] comprising determining dependencies among a plurality of firmware modules [option ROMs associated with devices] based on information about services imported [part of ROM header data structure] and exported [via register arguments] by each of the firmware modules [col.1, ll.51-56; col.7, ll.1-42; col.8, ll.6-46].

Patel did not disclose explicitly dispatching each module of the plurality of firmware modules in an order that satisfies the dependencies. Examiner had taken Official Notice that it is well known in the art to dispatch modules in an order based on dependencies, as the meaning of dependencies inherently involves an ordering [e.g., parent must come before child].

16. As to claim 51, Patel discloses, wherein the information about services imported and exported by a firmware comprises an export table [interrupt table] containing at least

one service provided by the firmware module [col.7, ll.1-29; col.8, ll.6-46; interrupts associated with calls].

17. As to claim 53, Patel discloses, wherein dispatching a module comprises saving a return address in a processor register [far return to POST; address saved in processor register as is well known in the art] and executing a beginning instruction of the module [e.g., performs device specific write-protection] [col.7, ll.1-29, ll.43-47].

18. In re claim 54, Stevens discloses a system [fig.2] comprising:

- A hardware component [e.g., 11] to perform a function [e.g., execute instructions].
- A volatile memory [13] that can store data after the volatile memory is initialized.
- A non-volatile memory [15, 20a] containing a BIOS including a BIOS core and a plurality of firmware modules [16, 17, n modules in 20a].
- Wherein two of the plurality of firmware modules [e.g., module to initialize CPU, module to initialize system memory] are to initialize hardware components [e.g., cpu, system memory] to perform the function [col.2, ll.4-11; col.3, ll.1-3].
- Said two of the plurality of firmware modules are to be dispatched before the volatile memory is initialized [col.3, ll.1-3].

19. Stevens did not disclose the situation where a hardware component is not present in the system.

20. Patel discloses a system [analogous to Stevens] wherein one of the two firmware modules is to initialize a hardware component [devices] that is not present in the system [fig.2; col.6, ll.10-47; if one of the hardware component is not present, steps 206-218 are repeated with one of the firmware module taken out of dispatched allocation map].

Art Unit: 2116

21. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Patel before him at the time the invention was made, to modify the system taught by Stevens to include the teachings of Patel, in order to obtain the claimed method and system, including wherein the initializing of the plurality of firmware modules further comprises executing a core module by determining a requirements configuration of the plurality of firmware modules appropriate to run [col.3, ll.40-48; run Stevens core module statically instead of via system memory to conserve memory resource]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enhance the robustness of BIOS operation [Patel: col.1, ll.51-56; e.g., Patel's teaching enhances Stevens' early initialization by enabling the determination of whether the system memory or required resources is present or not] while conserving memory resource.

22. As to claim 55, Stevens discloses, wherein the volatile memory is a RAM [col.4, 1.37].

23. As to claim 56, Stevens discloses, wherein the non-volatile memory is at least one of a ROM or a flash memory [col.5, ll.1-26].

24. Claims 45-47, 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Patel as applied to claim 42 above, and further in view of Ayers et al., US Patent 6353924, hereinafter Ayers.

25. Stevens and Patel taught each and every limitation of the claim as discussed above. Stevens and Patel did not disclose explicitly marking a data structure after dispatching a firmware module.

Art Unit: 2116

26. In re claim 45, Ayers discloses a method comprising marking a data structure [e.g., table] after dispatching a firmware module [e.g., block], wherein the data structure is to indicate whether the firmware module has been dispatched [col.4, ll.51-58].
27. It would have been obvious to one of ordinary skill in the art, having the teachings of Ayers, Stevens and Patel before him at the time the invention was made, to modify the system taught by Stevens and Patel to include the explicit well known data structure teachings of Ayers, as using data structures to record an event [e.g., dispatched firmware module] is very well known and suitable for use in the system of Stevens and Patel. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to record events and aid debugging efforts [Ayers: col.1, ll.1-30].
28. As to claim 46, Ayers discloses, wherein the data structure is a bit array [circular buffer] [col.4, ll.17-19].
29. As to claim 47, Ayers discloses, wherein the data structure is held in a processor register [col.4, ll.5-16].
30. As to claim 52, Ayers discloses each and every limitation as discussed above in reference to claims 45 and 47.
31. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Patel as applied to claim 48 above, and further in view Katayama et al., US Publication 20010007119, hereinafter Katayama.
32. Stevens and Patel taught each and every limitation of the claim as discussed above. Patel discloses scanning to find a module that operates with a hardware component present in the platform and invoking the function if such a module is found

Art Unit: 2116

[col.6, ll.10-48]. Stevens and Patel did not disclose explicitly the firmware modules being arranged in a daisy chain.

33. Katayama discloses a method comprises a daisy chain of [firmware] modules [e.g., 85, 91] [0107-0109].

34. It would have been obvious to one of ordinary skill in the art, having the teachings of Patel, Stevens and Katayama before him at the time the invention was made, to modify the system taught by Stevens to include the teachings of Patel and the explicit well known daisy chain teachings of Katayama, as using daisy chains to organize related objects [e.g., firmware module] is very well known and suitable for use in the system of Stevens. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enhance the robustness of BIOS operation [Patel: col.1, ll.51-56; e.g., Patel's teaching enhances Stevens' early initialization by enabling the determination of whether the system memory or required resources is present or not] and organize data that allows continuous access without the data being required to be stored in a continuous location [Katayama: 0109].

***Response to Arguments***

35. Applicant's stipulation that "dispatch" is "execute" changes the scope of the claims and obviates the previous objections to the drawings and rejections under 35 U.S.C. 112, first paragraph.

36. Applicant's arguments with respect to claims 42 and 48 have been considered but are moot in view of the new ground(s) of rejection.

37. Applicant's arguments discussed in the following have been fully considered but they are not persuasive.

Art Unit: 2116

38. Applicant argues that “fixed resources” would not necessitate importing or exporting to satisfy the requirement. Examiner disagrees and submits that the fixed resources demanded for operation may include device drivers of other devices to be imported [col.7, l.60 – col.8, l.5]. Moreover, such teaching implicitly indicates “dependencies among a plurality of firmware modules”.
39. Applicant argues that “information pertaining to whether the device may act as a boot device and to locate values related to defining resource requirements, which neither can be considered to be equivalent to ‘information about services... exported’”. Examiner disagrees and submits that the information indicates services that can be exported for at least booting purposes [col.8, ll.38-46].

40. Applicant argues that “these devices are necessarily present in order for the system to accomplish this task”. Examiner submits that the system initially does not know the whether the devices are present or not, which is why the devices are activated and deactivated to identify “any additional devices” [col.6, l.20].

41. As such, Applicant’s arguments are deemed not persuasive and the rejections are maintained.

***Conclusion***

42. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen  
August 14, 2007

REHANA PERVEEN  
SUPERVISORY PATENT EXAMINER  
8/29/07